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Research Article

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Self-Aligned Top-Gate Amorphous Indium Zinc Oxide Thin-Film Transistors Exceeding Low-Temperature Poly-Si Transistor Performance

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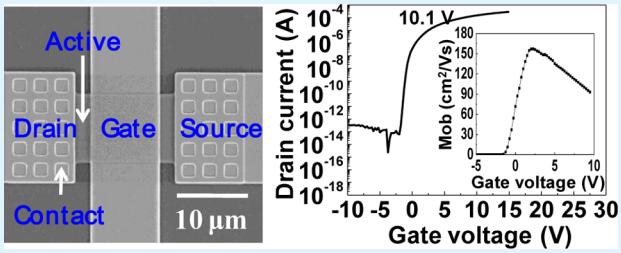
Supporting Information

ABSTRACT: Thin-film transistor (TFT) is a key component of active-matrix flat-panel displays (AMFPDs). These days, the low-temperature poly silicon (LTPS) TFTs are to match with advanced AMFPDs such as the active matrix organic light-emitting diode (AMOLED) display, because of their high mobility for fast pixel switching. However, the manufacturing process of LTPS TFT is quite complicated, costly, and scale-limited. Amorphous oxide semiconductor (AOS) TFT technology is another candidate, which is as simple as that of conventioanl amorphous (a)-Si TFTs in fabrication but provides much superior device performances to those of a-Si TFTs. Hence, various AOSs have been compared with LTPS for active channel layer of the advanced TFTs, but have always been found to be relatively inferior to LTPS. In the present work, we clear the persistent inferiority, innovating the device performaces of a-IZO TFT by adopting a self-aligned coplanar top-gate structure and modifying the surface of a-IZO material. Herein, we demonstrate a high-performance simple-processed a-IZO TFT with mobility of ~157 $cm^2\ V^{-1}\ s^{-1}$, SS of ~190 mV dec^{-1}, and good bias/photostabilities, which overall surpass the performances of high-cost LTPS TFTs.



KEYWORDS: *self-aligned top-gate structure, amorphous indium zinc oxide, thin-film transistor, N_2O plasma treatment, Ar plasma treatment*

INTRODUCTION

Thin-film transistor (TFT) is a key technology of active-matrix flat-panel displays (AMFPDs). TFTs are used for not only the pixel circuits but also the peripheral driving circuits integrated around the pixel array. Amorphous silicon (a-Si) TFTs have been used to be the pixel driver of active-matrix liquid-crystal displays (AMLCDs). However, high-resolution AMLCDs with over 300 pixel per inch are hard to be made using a-Si TFTs which have a low field-effect mobility (μ_{FE}) of 0.5 $cm^2\ V^{-1}\ s^{-1}$. Moreover, active-matrix organic light-emitting diodes (AMOLEDs) could not be realized with a-Si TFTs at all. Low-temperature poly silicon (LTPS) TFTs have thus been adopted to match with AMOLEDs, even though the manufacturing process of LTPS TFT is quite complicated, costly, and scale-limited. Hence, there have been growing needs to develop a low-cost and high-performance TFT technology that can replace LTPS-based ones. Amorphous oxide semiconductor (AOS) TFT technology was a candidate,[1−6] because the fabrication process of AOS TFTs is as simple as that of a-Si TFTs, whereas in fact the performance of AOS TFTs is much superior to that of a-Si TFTs. AOS TFT with indium gallium zinc oxide (IGZO) active channel has stably achieved μ_{FE} larger than 10 $cm^2\ V^{-1}\ s^{-1}$.[3] This value is enough to match for pixel circuits of high-resolution AMLCDs; however, it is still not sufficient to match any high frame rate display such as AMOLEDs or system-on-panel (SOP) applications. Amorphous indium zinc oxide (a-IZO) without Ga might be a promising material to meet the aforementioned situation, since it demonstrated higher mobility (~40 $cm^2\ V^{-1}\ s^{-1}$) than that of IGZO as a TFT channel; in fact the mobility tends to proportionally increase with In content.[4−11] The main problem of previously reported a-IZO TFTs was that other performance factors except μ_{FE} (such as subthreshold swing (SS), on/off current ratio, and bias stress stability) were inferior to those of IGZO TFTs in general. Moreover, the reported μ_{FE} of a-IZO TFTs is quite high, but not high enough to compete with that of LTPS TFTs (50−100 $cm^2\ V^{-1}\ s^{-1}$). In more details, conventional a-IZO TFTs were basically staggered (or inverted staggered) type devices using an undoped source/drain contact, which would cause a considerable contact and series resistances lowering μ_{FE} although the intrinsic channel mobilty is potentially higher.[12,13] Overlap area between the source/drain

Received: March 28, 2013
Accepted: July 3, 2013
Published: July 3, 2013

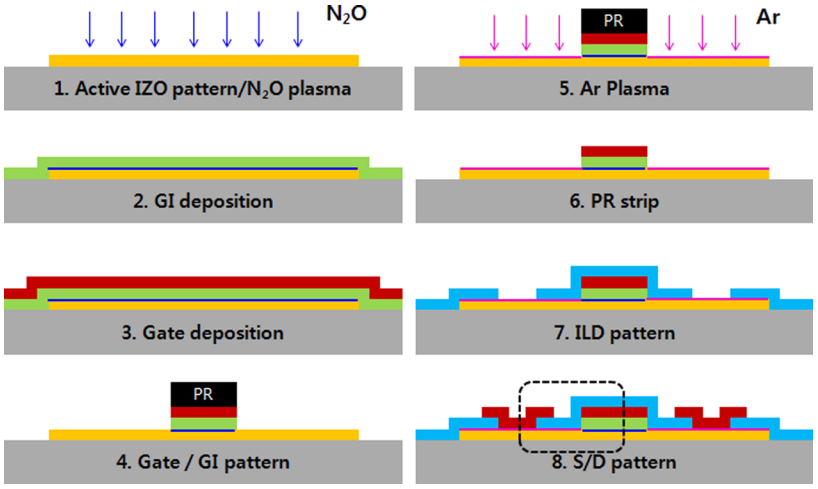


Figure 1. Process steps for the self-aligned top-gate IZO TFT as shown in schematic cross sections of the device. N_2O and Ar plasma-treated layers are respectively indicated by blue and pink lines in the device cross-section. ILD represents interlayer dielectric, GI is gate insulator, and PR means photoresist. Red represents Mo S/D/G layer.

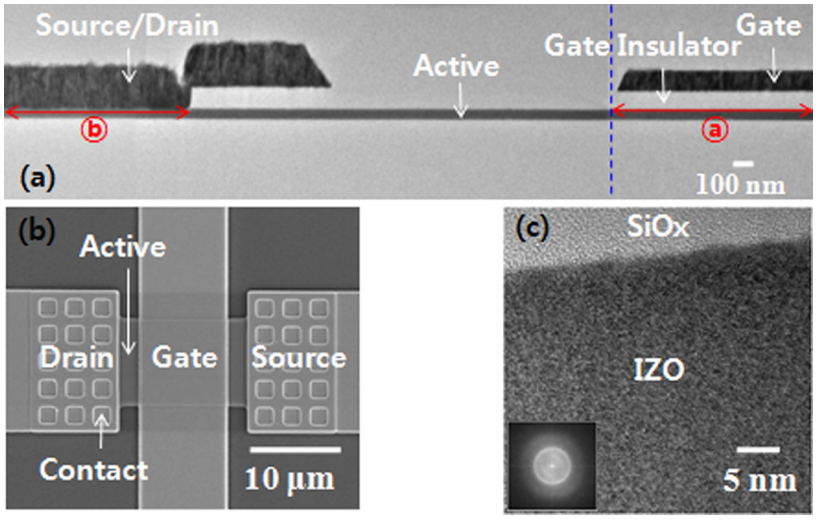


Figure 2. (a) Cross-sectional TEM image and (b) the plan-view SEM images of our self-aligned top-gate a-IZO TFT. Image in a represents the rectangular area of process step 8 in Figure 1. (Parts of S/D and channel regions are respectively annexed with two TEM images. The vertical dashed line near channel region indicates the annexation border of two TEM micrographs.) (c) TEM image and the corresponding SAED pattern (inset) of a-IZO active layer.

and gate electrodes in the staggered device causes both parasitic capacitance and degraded scalability, that bring difficulties in high-speed driving in high-resolution AMFPDs.[14] This staggered structure also causes back channel current which is the source of high off-current and large subthreshold swing. To solve the above problems of staggered structure, a few efforts were made on oxide TFTs adopting self-aligned top-gate structure. Morosawa et al. attempted a metal reaction process on IGZO active layer for lowering S/D contact resistance, whereas Chen et al. applied hydrogen plasma treatment on ZnO active layer to obtain low series resistance of S/D region,[15,16] although minor improvement was made in device performance.

In the present work, we clear the persistent issues of widely used staggered structure, adopting self-aligned coplanar top-gate structure for a high performance a-IZO TFT. Simultaneously, we increased the In content of IZO channel (particularly at the contact region) to maximize the mobility, also increasing the surface O content of the channel film as well to enhance the on/off ratio and stability. The novelty of our work is in that we sequentially used two different plasma processes for the improvement of the IZO channel and S/D contact region in that order, whereas other previous works investigated only individual plasma process for channel or S/D contact in their researches. As a result, we here demonstrate a high-performance simple-processed (low cost) a-IZO TFT with the mobility of ~157 $cm^2\ V^{-1}\ s^{-1}$, SS of ~190 mV dec^{-1}, and good bias/photostabilities, which are overall surpassing the performances of high-cost LTPS TFTs. The mobility value is regarded to be the most superior among previously reported ones of AOS TFTs, to the best of our limited knowledge.[7,8,10,17,18]

EXPERIMENTAL SECTION

Figure 1 shows the detailed process steps for our self-aligned device. 6-in. glass wafers were used as substrates. The self-aligned top-gate a-IZO TFTs were fabricated using the standard semiconductor processes. (1) The 30 nm or 50 nmthick a-IZO films were deposited

dx.doi.org/10.1021/am401128p | ACS Appl. Mater. Interfaces 2013, 5, 6990−6995

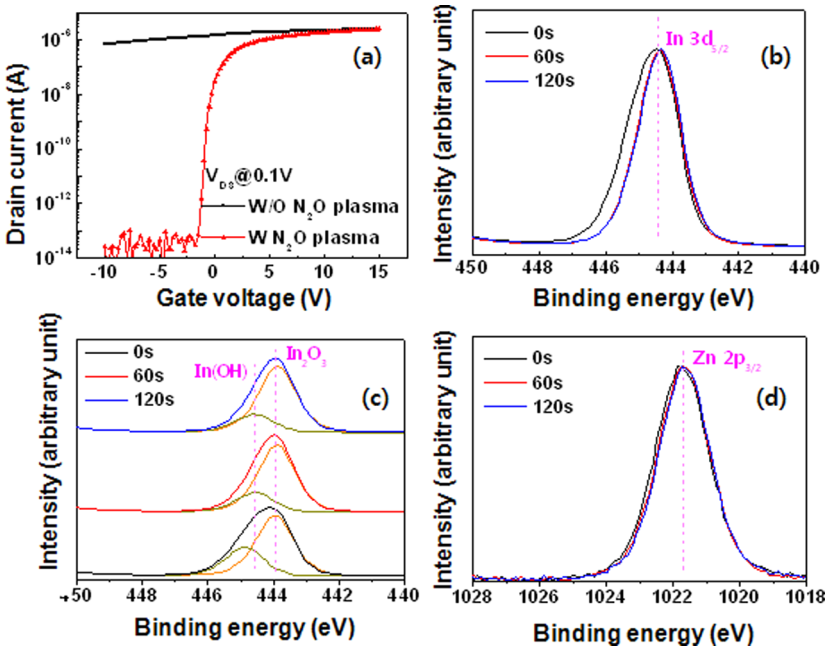


Figure 3. (a) Transfer curves of 50 nm thick a-IZO TFTs without (w/o) and with (w) N_2O plasma treatment of 120 s. The width and length of TFT are 10 and 10 μm, respectively. (b) Normalized XPS peaks for In $3d_{5/2}$ of IZO surface treated by N_2O plasma for 0, 60, and 120 s. (c) Those peaks are analyzed with subpeaks to identify their chemical states. (d) Normalized XPS peaks for Zn $2p_{3/2}$ are shown identical in binding energy position regardless of N_2O plasma treatment.

as active layers on the respective substrates using radio frequency (RF) magnetron sputtering at room temperature. The sputtering gas was the mixture of Ar and O_2 of 100:1 flow rate. Two kinds of sputtering target were used for the a-IZO deposition: targets with 1:1 In:Zn atomic ratio and with 9:1 In:Zn atomic ratio. Active layers were patterned by wet etching. On the active layer pattern, the N_2O plasma treatment was implemented for 120 s and (2) subsequentially a 100 nm thick SiOx gate insulator was deposited without vacuum breaking. N_2O plasma conditions were 50 W RF power, 550 mTorr working pressure, and 150 °C substrate temperature. SiOx gate insulator was deposited using plasma enhanced chemical vapor deposition (PECVD) at the process condition such as RF power of 60 W, RF frequency of 380 kHz, working pressure of 550 mT, $SiH_4/N_2O/N_2$ gas flow rates of 160/1420/240 sccm and deposition temperature of 150 °C. (3) On the gate insulator, 100 nm thick molybdenum (Mo) gate metal was sputter-deposited at room temperature. (4) The Mo gate and the SiOx gate insulator were then patterned by continuous dry etching. (5,6) After the patterning of the gate and gate insulator, we treated source/drain contact region by Ar plasma for 60 s. Ar plasma treatment conditions were 50 W RF power, 200 mTorr working pressure and 150 °C substrate temperature. (7) After then, 150 nm thick SiOx interlayer dielectric (ILD) was deposited by PECVD at 150 °C and then patterned by dry etching. (8) Finally, 200 nm thick Mo source/drain metal was sputtered at room temperature and then patterned by dry etching.

Electrical characteristics were measured by using Keithley 4200 semiconductor parameter analyzer under ambient conditions. RBS analysis was conducted using 450 keV He^+ ions at an incident angle of 50° and a backscattering angle of 73.5°. Hitachi 7600 operating at 300 kV was used for TEM analysis. Surface analysis by XPS was performed by a PHI Quantum 2000 which employs an Al Kα (1486.6 eV) X-ray source operating at 15 kV and 25 W. The takeoff angle was 45°.

RESULTS AND DISCUSSION

As shown in Figure 1 and the Experimental Section, N_2O (blue arrows) and Ar (pink arrows) plasma treatments are respectively introduced on IZO channel (blue layer) and source/drain contact region (pink layer) as our systematic approaches to achieve high device performances exceeding those of LTPS TFTs. Figure 2a displays the dashed rectangular area of the process step number 8 in Figure 1 as a cross-sectional transmission electron microscopy (TEM) image of our a-IZO TFT device (annexed images of source/drain (S/D) and channel regions in same scale), whereas Figure 2b shows the plan view of our device as the scanning electron microscopy (SEM) image where IZO active channel area and Mo S/D contact holes are noted. Figure 2c and its inset respectively show the TEM image and selective area electron diffraction (SAED) pattern obtained from IZO film with an In:Zn content of 9:1. According to the diffuse-ring type SAED pattern, it is highly likely that our IZO layer has an amorphous phase.[19,20]

Figure 3a shows the two drain current−gate voltage (I_D−V_G) transfer curves that were obtained from IZO TFTs prepared without and with N_2O plasma treatment on the IZO surface (e.g., the channel region denoted as a in Figure 2a). Without N_2O plasma treatment, the transfer curve shows almost conducting regardless of V_G change, but it changes to show V_G-dependent field-effect with the 120 s plasma treatment displaying a typical transistor behavior. It is because as-deposited initial a-IZO has quite a conductive surface by itself with a high density of oxygen vacancies. Besides, H atom incorporation into the a-IZO layer during gate insulator (GI) deposition (plasma-enhanced chemical vapor deposition, SiO_2 PECVD) would more increase the active layer conductivity,[6] harming any suitable switching performance of the TFT. The N_2O plasma treatment provides oxygen atoms to the O-deficient surface, so that the conductive a-IZO surface recovers its semiconducting properties.[21] The N_2O plasma effects on the IZO surface were analyzed with X-ray photoelectron spectroscopy (XPS) as shown in Figures 3b∼d. According to XPS results for In $3d_{5/2}$ and Zn $2p_{3/2}$ signals,[22−24] In−O binding significantly changes to form more stoichiometric In_2O_3 phase with a longer plasma treatment time while Zn−O binding in

IZO has been little changed with the N_2O surface treatment time. As a result, more electrically resistive phase of semiconducting IZO with a lower density of oxygen vacancies is expected with the plasma treatment. As the plasma time gets longer, more In_2O_3 but less In(OH) compound would be achieved (Figure 3c). Table 1 summarizes the plasma time-dependent In compound variations as analyzed by XPS, according to which in fact the effective In_2O_3 formation is almost saturated within only 60 s of plasma treatment. In the Supporting Information, we also prepared Table S1 for ZnO compound information with regards to the plasma treatment time.

Table 1. Concentration of In Compounds Estimated by Two Individual Sub-peaks Resolved from In $3d_{5/2}$ Signals

N_2O plasma	component	positive	concentration (%)
as-fab	In_2O_3	444.3	69.5
	In(OH)	445.3	30.5
60 s	In_2O_3	444.5	78.7
	In(OH)	445.1	21.3
120 s	In_2O_3	444.4	80.1
	In(OH)	445.1	19.9

The source/drain (S/D) contact of a-IZO (denoted as region b in Figure 2a) was made ohmic through argon (Ar) plasma treatment. Because it is known that the conductivity of IGZO layer increases through Ar plasma treatment,[25,26] we expected that Ar plasma could increase the conductivity of a-IZO layer in a similar manner reducing the contact resistance in the S/D region. Moreover, in view of our self-aligned coplanar device structure (see step 8 in Figure 1), the Ar plasma-induced ohmic regions are directly connected to the a-IZO channel, so that the series resistance between the channel and source/drain would also be reduced. Therefore, the Ar plasma treatment would reduce the both resistances: series and contact. The plot in Figure 4a shows the Ar plasma effects on the sheet resistance (R_s) of 50 nm thick a-IZO, which completely decreases to ~0.8 kΩ/□ within 3 min treatment. Cross-sectional TEM images of the a-IZO layer are also shown in Figure 4b; the channel region a appears uniform without any contrast change while the source/drain contact region b displays a 5 nm thin gray strip at the top surface as an indicator of In-rich region induced by Ar plasma treatment. Such microscopic observation of Ar plasma treatment on the a-IZO surface was supported by surface composition analysis using Rutherford backscattering spectrometry (RBS) in Figure 4c, which displays the In content increase at the surface of a-IZO film after 2 min Ar plasma treatment as compared with the spectra before the treatment. Inset shows our detector angle for RBS measurement, which was set up to resolve the plasma-treated 5 nm thickness. (The relative compositions of zinc and oxygen appear still unchanged at the surface as seen in Supporting Information, Figure S1). Finally, as a direct evidence experiment, contact resistance measurements were implemented by using Kelvin contact pattern (details are shown in Figure S2 in the Supporting Information).[27−29] Figure 4d shows the current−voltage (I−V) curves obtained from the molybdenum (Mo)/a-IZO contact areas of the Ar plasma-treated film, which were varied from 4 × 4 to 10 × 10 μm^2. All contacts exhibited ohmic behavior and the specific contact resistance was estimated to be 6.02 × 10^{-6} Ωc m^2 (linear regression value as shown in Figure S3 in the Supporting Information), whereas other samples without Ar plasma treatment showed nonohmic behavior and low level conductivities (see other I−V curves in Figure S4 in the Supporting Information). According to above RBS spectra and electrical measurements, we regard that the plasma-induced ion bombardment may cause the bond breaking of weak In−O

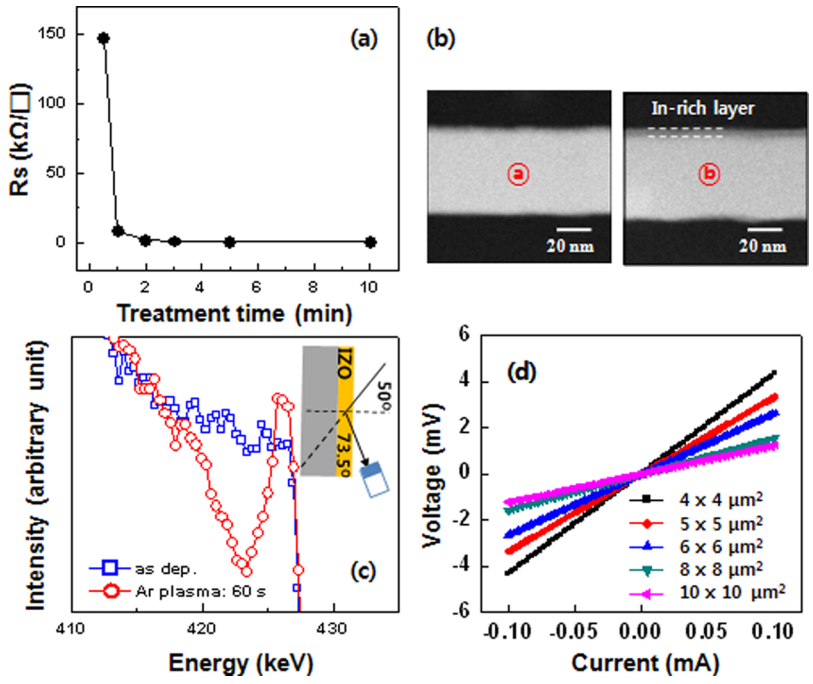


Figure 4. (a) Sheet resistance of a 50 nm thick a-IZO thin film as a function of Ar plasma treatment time. (b) Cross-sectional TEM images showing a detail of a-IZO layer surface in (a) channel region and (b) S/D region. (c) RBS spectra of a-IZO thin film without and with Ar plasma treatment. (d) Kelvin contact pattern-adopting I−V curves showing ohmic results after 60 s Ar plsama treatment; various contact sizes were taken to estimate a specific contact resistance.

dx.doi.org/10.1021/am401128p | ACS Appl. Mater. Interfaces 2013, 5, 6990−6995

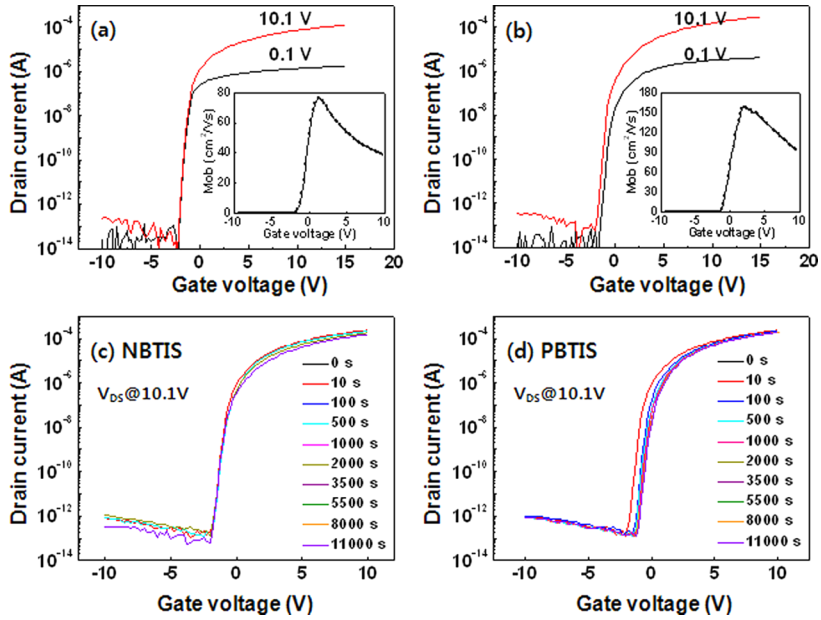


Figure 5. Transfer curves of a-IZO TFTs with (a) 30 nm thick and (b) 50 nm thick a-IZO active layers. The 0.1 and 10.1 V in the figures mean the drain−source voltage during the current−voltage measurements. (c, d) The a-IZO TFTs with 50 nm thick IZO went through (c) NBTIS and (d) PBTIS tests for maximum 11 000 s. After the illumination temperature stress, the transfer curves were measured at the drain−source voltage of 10.1 V as shown in the figures.

bonds of a-IZO films and also cause In-segregation at the top surface. Surface In segregation is very likely because Ar ions may more effectively transfer their kinetic energy and momentum to O than to heavy In atoms, so that the O atoms are recoiled behind the surface. Right behind the surface, more O and less (deficient) In contents would exist in In/O ratio but RBS does not well resolve O signal, whereas it is particularly sensitive to heavy elements such as In (as noted in the RBS spectra of Figure 4c for In and Figure S1 in the Supporting Information for O). This surface In content increases the conductivity of a-IZO films so much that energy barrier thickness between a-IZO and Mo might be narrow enough to cause charge carrier tunneling for low contact resistance.

Images a and b in Figure 5 respectively show the transfer curves of our TFTs with 30 and 50 nmthick a-IZO active layers, which has the same 9:1 In:Zn ratio for their composition. The channel width/length ratio was 10/10 and the respective insets display the V_G-dependent saturation mobility (μ_{FE}) plots of our TFTs, according to which 50 nm thick a-IZO device demonstrate 157 cm^2/ V s as a superior value to that (78.0 cm^2/V s) of the other device with 30 nm thin a-IZO, whereas their off current levels and threshold voltages (V_{TH}) are similar each other. This suggests that the channel layers are fully depleted under gate bias in the off-state region but the on-current level of the TFT with 50 nm thick a-IZO is higher than that of the other with 30 nm thick a-IZO, which means that an average active channel thickness should be larger in 50 nm thick a-IZO than in 30 nm thick one. The saturation mobility shows its peak but tends to decrease with V_G because transport electrons experience more scattering to dielectric/channel interface as V_G increases. Basically, 9:1 In:Zn composition makes the In-rich layer so conductive that under the accumulation voltage (on state) the active channel thickness may not only be the accumulation layer (Debye thickness) but also somewhat extend to the region below the top accumulation thickness. Table S2 in the Supporting Information summarizes μ_{FE}, subthreshold slope S, and V_{TH} values which are extracted from the transfer curves of three oxide TFTs with 30 nm thick (1:1 = In:Zn), another 30 nm thick (but 9:1), and 50 nm thick (9:1) a-IZO layers. SS values were less than 0.2 V/dec for all a-IZO TFTs. The μ_{FE} values of the 9:1 In:Zn a-IZO TFT was higher than that (~16 cm^2 V^{-1} s^{-1}) of the 1:1 In:Zn a-IZO TFT as we expect, because less In content makes the active layer less condcutive. The μ_{FE} over 100 $cm^2V^{-1}s^{-1}$ has ever been obtained from a polycrystalline Zn-free In_2O_3 TFT with a self-assembled superlattice dielectric as its gate insulator of high cost, but showing a poor On/OFF switching ratio of only 1×10^5.[30] Therefore, our self-aligned top-gate a-IZO TFT with 9:1 In:Zn is regarded as the most excellent device among AOS TFTs reported until recent years,[17,18] maintaining the highest μ_{FE} (157.2 cm^2 V^{-1} s^{-1}), small SS of 0.19 V/dec, V_{TH} near 0 V, and switching ratio greater than 1×10^9. According to the transfer curve plots in Figure S5a−d in the Supporting Information, these device performance values are uniformly achieved across the 6 in. glass wafer. Regardless of different channel width/length (W/L) ratio and locations, more than 10 IZO TFTs keep the similar mobility, V_{TH}, and SS value in each device. In addition, it is also noted that our a-IZO TFTs do not use any special gate insulator of high cost rather using a conventional SiOx gate insulator which keeps low production cost.

As our final experiment, electrical- and photostabilities of our devices were tested by imposing negative/positive bias illumination temperature stresses (NBTIS/PBTIS) on the devices for various periods (up to 11000 s); bias voltages for gate, drain and source during the NBTIS were ±20, 10 and 0 V, respectively, and the illumination/temperature condition was 3000 cd/m^2 white light onto the top opaque Mo gate of our a-IZO TFTs at 60 °C. When transfer curves were measured at a drain−source voltage of 10.1 V for the device with 50 nm thick layer after the NBTIS, little V_{TH} shift was observed along with

nearly identical S values as shown in Figure 5c. Whereas the V_{TH} shift of 1.0 V was observed after the PBTIS (Figure 5d), this V_{TH} shift was small and comparable with the previous reports.[31−35] Because these NBTIS/PBTIS conditions were incomparably more severe than the normal operation conditions of AMOLEDs, our a-IZO TFTs are regarded stable enough even for the backplane device of commercial AMOLED. As a minor result of electrical stability test, hysteresis behavior was also observed as shown in Figure 6S in the Supporting Information, where only a little gate hysteresis is seen from our 30 and 50 nm thick a-IZO channel TFTs.

CONCLUSION

In summary, we adopted high In content (9:1 In:Zn) a-IZO as the active material to fabricate a high mobility amorphous oxide TFTs, for which self-aligned top-gate coplanar structure was developed with N_2O plasma-treated channel and Ar plasma-treated S/D, to improve the active channel performance and to reduce the serial/contact resistance. Our device demonstrated a high performance with the mobility of ∼157 $cm^2 V^{-1} s^{-1}$, SS of ∼190 mV dec^{-1}, and good bias/photostabilities, which overall exceed the performances of LTPS TFTs. We thus conclude that our low-cost self-aligned a-IZO TFT with coplanar archetecture is promising enough to compete with the high cost LTPS TFT backplane for AMOLED. The mobility value is particularly regarded to be the most superior among previously reported ones of AOS TFTs, to the best of our limited knowledge.

ASSOCIATED CONTENT

Supporting Information

Full RBS spectra, kelvin contact pattern, specific contact resistance, nonohmic behavior, TFT uniformity, hysteresis behavior, estimated concentration of ZnO, and device parameters. This material is available free of charge via the Internet at http://pubs.acs.org.

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Notes

The authors declare no competing financial interest.

ACKNOWLEDGMENTS

Authors acknowledge the financial support from NRF (NRL program, 2012-0000126) and BK21 Project.

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